

FIG. 1

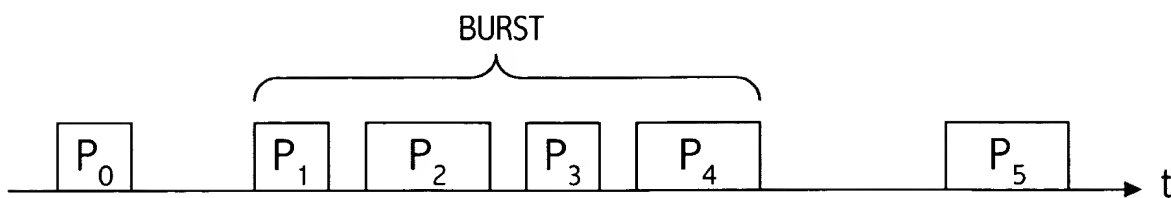


FIG. 2

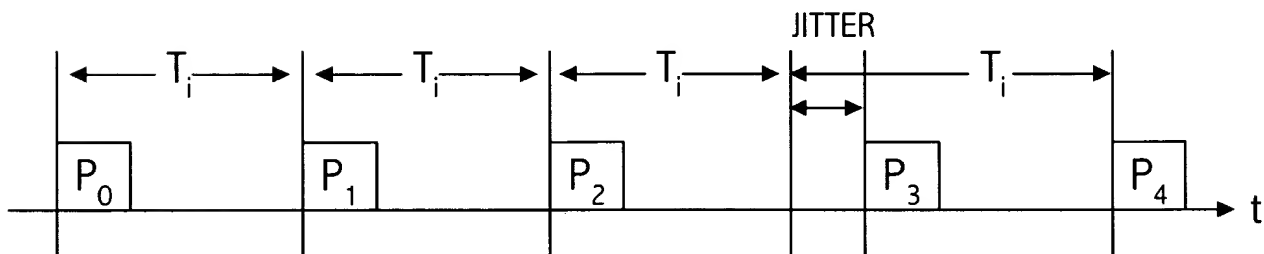


FIG. 3

09714341-111600

I	T	SLOT	RATE	LENGTH
0	2	1	2	3
1	3	1	0	1
1	2	5	4	5

FIG. 4

SLOT	PRECALC SCHEDULE $I_0$	PRECALC SCHEDULE, $I_1$
0	0000	0000
1	0010	0001
2	0000	0000
3	0010	0000
4	0000	0000
5	0010	0000

FIG. 5

I	T	SLOT
0	2,3	1
1	1,2,3	2
2	1,3	1

FIG. 6

SLOT	PRECALC SCHEDULE $I_0$	PRECALC SCHEDULE, $I_1$	PRECALC SCHEDULE, $I_2$
0	0000	0000	0000
1	0011	0000	0000
2	0000	0111	0000

FIG. 7

009747-1-11600

SLOT	PRECALC SCHEDULE $I_0$	PRECALC SCHEDULE, $I_1$	PRECALC SCHEDULE, $I_2$	PRECALC SCHEDULE, $I_3$
0	0111	1001	0000	0000
1	0000	1001	1110	0000
2	1100	0011	0000	0000

FIG. 8

SLOT 0

I \ T	0	1	2	3
0	0	X	X	X
1	1	0	0	1
2	0	0	0	0
3	0	0	0	0

SLOT 1

I \ T	0	1	2	3
0	0	0	0	0
1	X	0	0	X
2	1	1	1	0
3	0	0	0	0

SLOT 2

I \ T	0	1	2	3
0	X	X	0	0
1	0	0	X	X
2	0	0	0	0
3	0	0	0	0

 ROUND ROBIN POSITION  
 GRANTED REQUESTS

FIG. 9

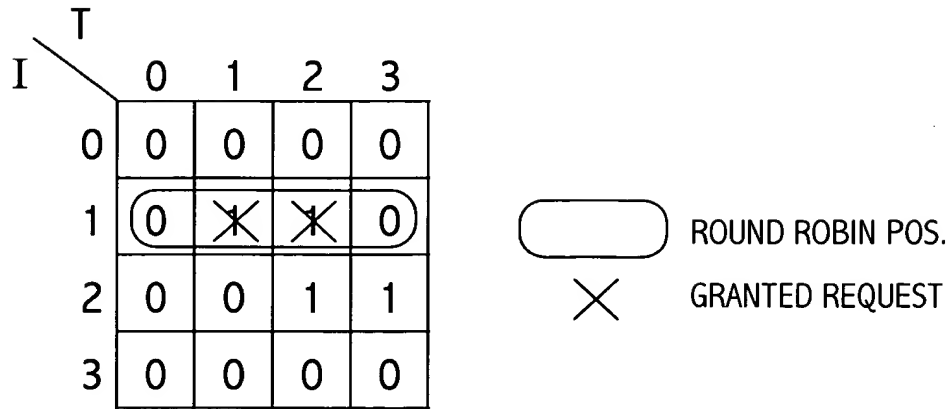


FIG. 10

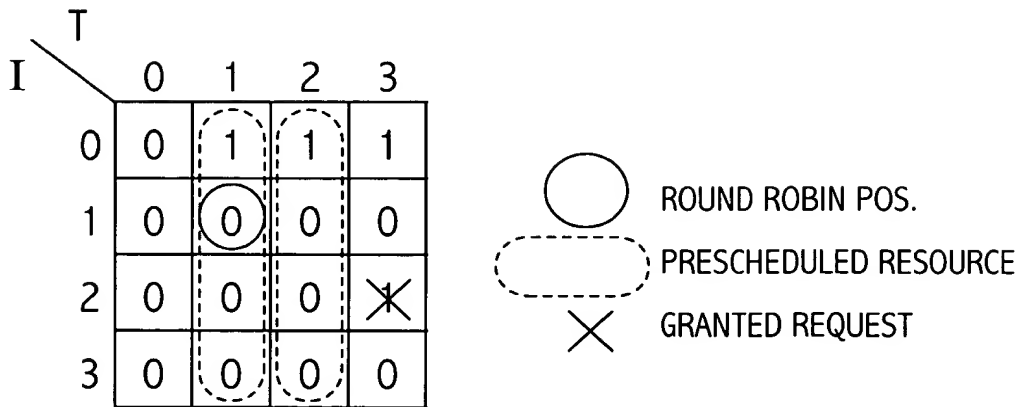


FIG. 11

009TTF"TFETZ60

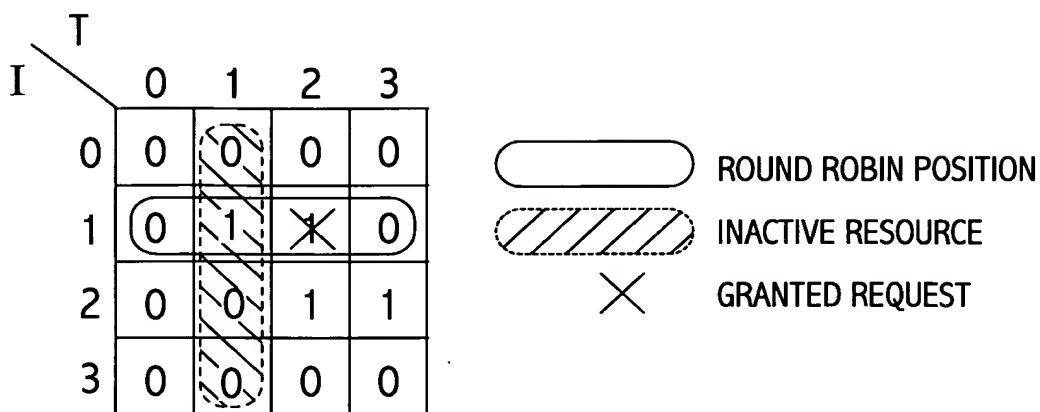


FIG. 12

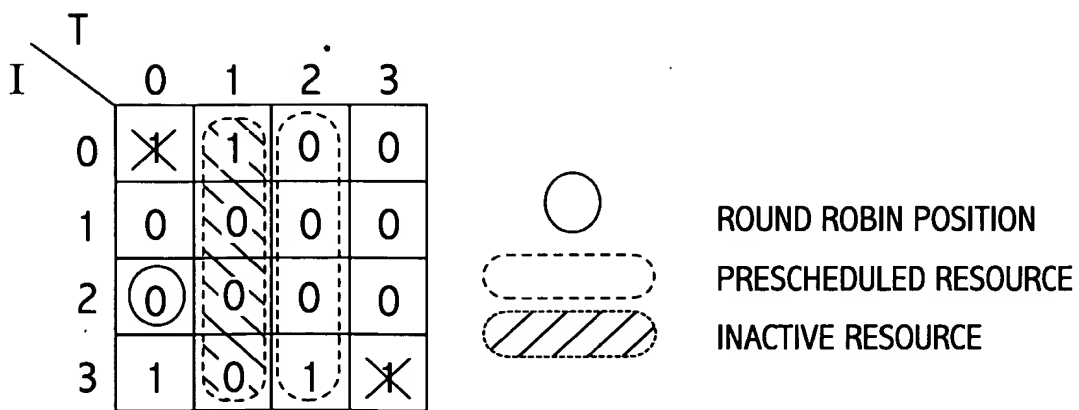


FIG. 13

009744341-11600

	Regular Requests				Prescheduled Requests			
	Output Port 0	Output Port 1	Output Port 2	Output Port 3	Output Port 0	Output Port 1	Output Port 2	Output Port 3
REQUEST VECTOR 0	1	1	0	0	0	0	0	0
REQUEST VECTOR 1	0	0	0	0	0	1	1	0
REQUEST VECTOR 2	0	0	0	0	0	0	1	1
REQUEST VECTOR 3	1	0	1	1	0	0	0	0

FIG. 14



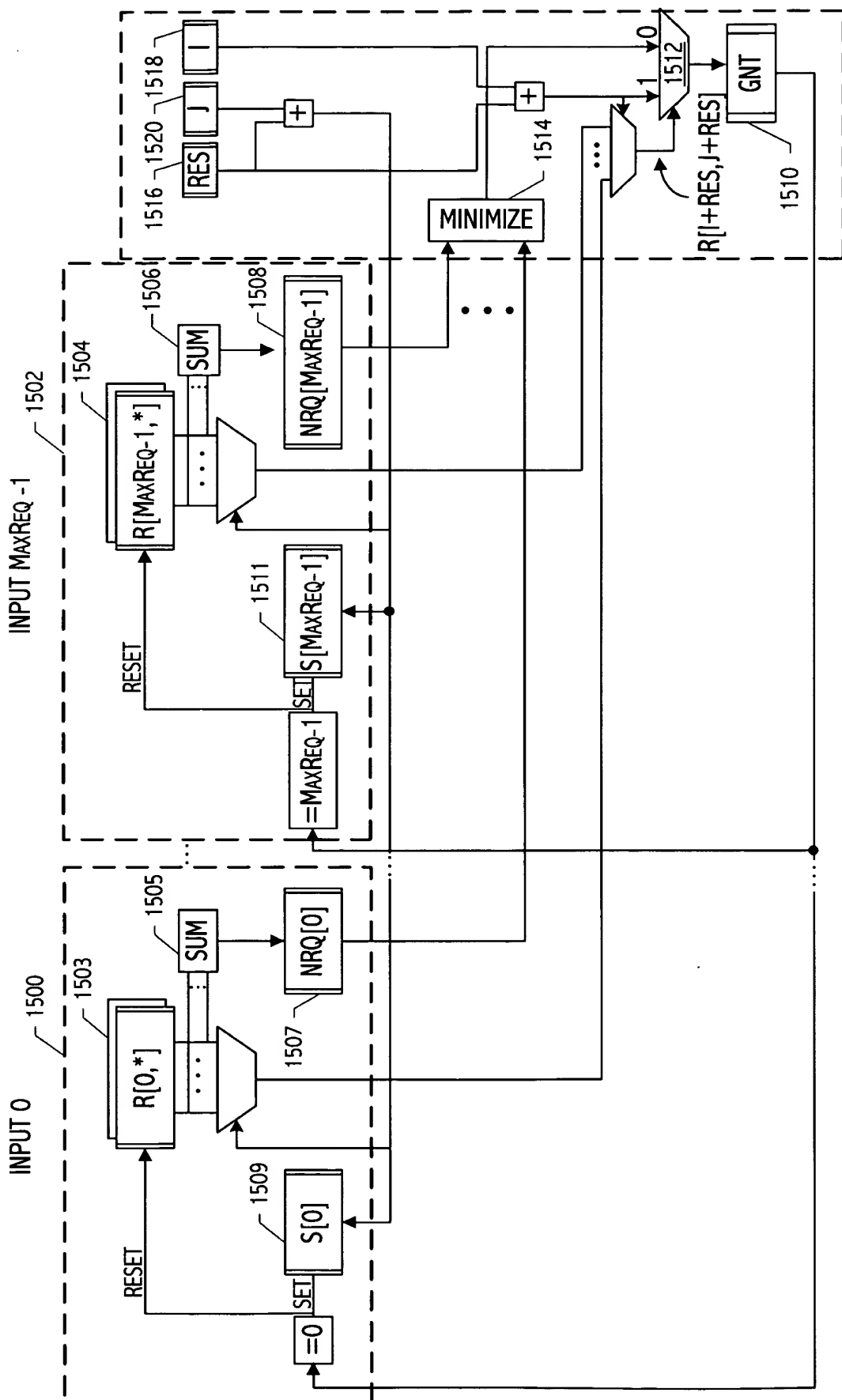


FIG. 15



FIG. 16

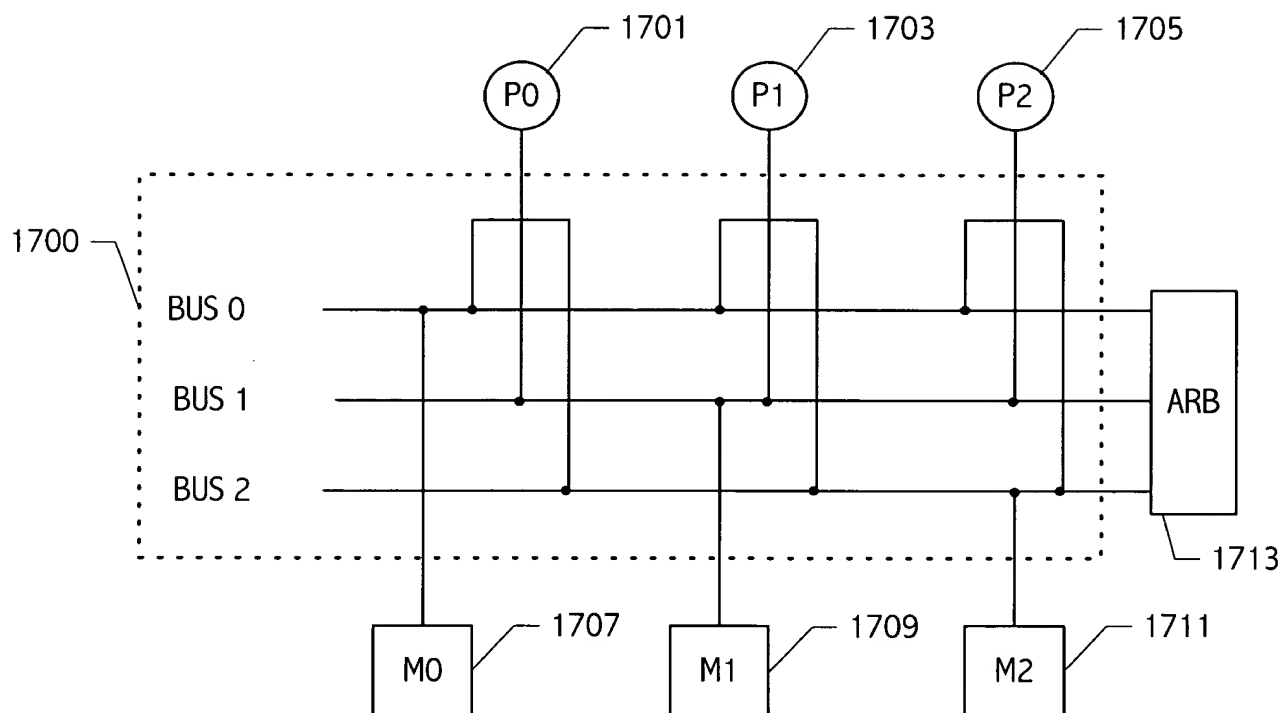


FIG. 17